a plurality of ports configured for transferring data packets;

an external memory interface configured for transferring the data packets between the network switch and an external memory, the external memory interface including a scheduler for selectively assigning memory access slots ~~of the external memory interface~~ to ports ~~based on respective programmable information entries~~ for access to the external memory, wherein

selectively assigning memory access slots by the scheduler is based on respective programmable information entries,

the external memory interface includes an assignment table memory for storing the respective programmable information entries, and

the programmable information entries are stored in the assignment table memory by an external controller.

Claims 2 and 3 (Canceled)

4. (Previously Presented) The network switch according to claim 1, wherein each programmable information entry includes a port operation code, and the scheduler sets the operation of each of the ports based on the port operation code.

5. (Previously Presented) The network switch according to claim 4, wherein the port operation code includes one of a read bit and a write bit, the scheduler selectively assigning each of the memory access slots as one of a read slot and a wire slot, based on the corresponding port operation code.

6. (Previously Presented) The network switch according to claim 1, wherein the programmable information entries include a sequence of memory access slot assignments, the scheduler assigning the memory access slots as a continuously repeating sequence based on the sequence of memory access slot assignments.

7. (Previously Presented) The network switch according to claim 6, wherein one of the programmable information entries includes a wrap-around bit at an end of the sequence of memory access slot assignments, the scheduler returning to a first memory access slot of the sequence of memory access slot assignments upon detecting the wrap-around bit.

8. (Previously Presented) The network switch according to claim 1, wherein the assignment table memory is a RAM.

9. (Previously Presented) The network switch according to claim 1, wherein the assignment table memory is a group of registers.

10. (Previously Presented) The network switch according to claim 1, wherein each programmable information entry includes a plurality of memory access slot assignments, the scheduler selecting one of the plurality of memory access slot assignments based on one or more detected conditions.

11. (Previously Presented) A method of assigning memory access slots in a network switch to a plurality of network switch ports, each configured for transferring data packets to an external memory, the method comprising:

storing programmed memory access slot assignment information into a memory;

selectively assigning memory access slots to the respective network switch ports based on the programmed memory access slot assignment information;

selectively assigning memory access slots to the respective network switch ports based on the programmed memory access slot assignment information;

selecting a slot-to-port assignment configuration from the programmed memory access slot assignment information; and

writing the selected slot-to-port assignment configuration from the memory to an assignment configuration memory within the network switch, the selectively assigning step including assigning the memory access slots to the respective network switch ports based on the selected slot-to-port assignment configuration stored in the assignment configuration memory, wherein

the storing step comprises setting each slot-to-port assignment within the slot-to-port assign configuration to include one of a read and a write bit for indicating whether a corresponding memory access slot is one of a read and write slot.

Claims 12 and 13 (Canceled)

14. (Previously Presented) A method of assigning memory access slots in a network switch to a plurality of network switch ports, each configured for transferring data packets to an external memory, the method comprising:

storing programmed memory access slot assignment information into a memory;

selectively assigning memory access slots to the respective network switch ports based on the programmed memory access slot assignment information;

selecting a slot-to-port assignment configuration from the programmed memory access slot assignment information; and

writing the selected slot-to-port assignment configuration from the memory to an assignment configuration memory within the network switch, the selectively assigning step including assigning the memory access slots to the respective network switch ports based on the selected slot-to-port assignment configuration stored in the assignment configuration memory, wherein

the storing step comprises setting the slot-to-port assignment configuration as a repeating sequence of an N number of memory access slot assignments.

15. (Previously Presented) A method of assigning memory access slots in a network switch to a plurality of network switch ports, each configured for transferring data packets to an external memory, the method comprising:

storing programmed memory access slot assignment information into a memory;

selectively assigning memory access slots to the respective network switch ports based on the programmed memory access slot assignment information;

selecting a slot-to-port assignment configuration from the programmed memory access slot assignment information; and

writing the selected slot-to-port assignment configuration from the memory to an assignment configuration memory within the network switch, the selectively assigning step including assigning the memory access slots to the respective network switch ports based on the selected slot-to-port assignment configuration stored in the assignment configuration memory, wherein

the storing step includes storing into the slot-to-port assignment configuration a wrap-around bit that returns the sequence of an N number of memory access slot assignments to a first memory access slot at a start of the sequence of an N number of memory access slot assignments from an "Nth" memory access slot.

Claims 16. (Canceled)

17. (Currently Amended) A switched network system comprising:

a first memory for storing a plurality of programmable system settings;

a second memory for storing data packets;

a network switch having a plurality of ports configured for transferring the data packets, the network switch including:

(1) an external memory interface configured for transferring data packets between the network switch and the second memory; and

(2) a scheduler for selectively assigning memory access slots to each of the ports for access to the second memory, the selectively assigning memory access slots to each of the ports being based on a selected one of the plurality of programmable system settings stored in the first memory; and

a system controller for supplying the selected one of the plurality of programmable system settings to the network switch.

18. (Previously Presented) The switched network system according to claim 17, wherein the external memory interface includes a memory access slot assignment table memory.

19. (Previously Presented) The switched network system according to claim 17, wherein the plurality of programmable system settings include a port operation code, and the scheduler sets the operation of each of the ports based on the port operation code.

20. (Previously Presented) The switched network system according to claim 19, wherein the port operation code includes one of a read bit and a write bit causing the scheduler to assign the memory access slots as read and write slots, respectively.

21. (Previously Presented) The switched network system according to claim 17, wherein the plurality of programmable system settings include a sequence of an N number of memory access slot assignments that is continuously repeated by the scheduler in assigning the memory access slots.

22. (Previously Presented) The switched network system according to claim 21, wherein the plurality of programmable system settings include a wrap-around bit at an end of the sequence and the scheduler returns to a first memory access slot at a start of the sequence upon detecting the wrap-around bit.

23. (Previously Presented) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a RAM.

24. (Previously Presented) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a group of registers.

25. (Original) The switched network system according to claim 17, wherein the first memory is an EEPROM.